ABSTRACT OF THE DISCLOSURE

Provided is a digital duty cycle correction circuit and method for a multi-phase clock, in which duty cycle correction information of an input clock signal is stored in a power save state of a system by adopting a digital correction method in a duty cycle correction method for a multi-phase clock and phase information of the input clock signal is held constant during duty cycle correction of the input clock signal by correcting duty cycles of the input clock signal by changing the falling edge of the clock without changing the rising edge of the input clock signal during duty cycle correction of the input clock signal, thereby correcting the multi-phase clock. To this end, the digital duty cycle correction circuit includes a clock delay means that takes the form of a shunt capacitor-inverter, a clock generation means including a clock rising edge generation circuit and a clock falling edge generation circuit, and a digital duty cycle detection means including integrators, a comparator, and a counter/register.